IN THE CLAIMS

We claim:

1. (Original) A process comprising:

in a substrate, forming a first isolation structure spaced-apart from a second isolation structure;

forming an emitter stack between the first and second isolation structures;

in the substrate, forming a self-aligned recess between the emitter stack and the first isolation structure; and

forming a bipolar junction transistor between the first and second isolation structures.

2. (Original) The process according to claim 1, further including:

implanting a self-aligned collector tap in the self-aligned recess.

3. (Currently Amended) A [[The process according to claim 1,]] comprising:

in a substrate, forming a first isolation structure spaced-apart from a second isolation structure;

forming an emitter stack between the first and second isolation structures;

in the substrate, forming a self-aligned recess between the emitter stack and the first isolation structure; and

forming a bipolar junction transistor between the first and second isolation structures,

wherein forming a self-aligned recess further includes:

patterning a mask that exposes a portion of the first isolation structure, a portion of the emitter stack, and a portion of the substrate located between the first isolation structure and the emitter stack; and

etching the self-aligned recess with an etch recipe that is more selective to the first isolation structure and the emitter stack than to the substrate.

4. (Currently Amended) A [[The process according to claim 1,]] comprising:

in a substrate, forming a first isolation structure spaced-apart from a second isolation structure;

forming an emitter stack between the first and second isolation structures;

in the substrate, forming a self-aligned recess between the emitter stack and the first isolation structure; and

forming a bipolar junction transistor between the first and second isolation structures,

wherein forming a self-aligned recess further includes:

patterning a mask that exposes a portion of the first isolation structure, a portion of the emitter stack, and a portion of the substrate located between the first isolation structure and the emitter stack; and

anisotropically etching the self-aligned recess with an etch recipe that is more selective to the first isolation structure and the emitter stack than to the substrate.

5. (Currently Amended) A [[The process according to claim 1,]] comprising:

in a substrate, forming a first isolation structure spaced-apart from a second isolation structure;

forming an emitter stack between the first and second isolation structures;

in the substrate, forming a self-aligned recess between the emitter stack and the first isolation structure; and

forming a bipolar junction transistor between the first and second isolation structures,

wherein implanting a self-aligned collector tap in the self-aligned recess includes:

patterning a mask that exposes at least a portion of the first isolation structure and the emitter stack; and

implanting a dopant into the substrate that is exposed by the self-aligned recess.

6. (Currently Amended) A [[The process according to claim 1,]] comprising:

in a substrate, forming a first isolation structure spaced-apart from a second isolation structure;

forming an emitter stack between the first and second isolation structures;

in the substrate, forming a self-aligned recess between the emitter stack and the first isolation structure; and

forming a bipolar junction transistor between the first and second isolation structures,

wherein implanting a self-aligned collector tap in the self-aligned recess includes:

patterning a mask that exposes at least a portion of the first isolation structure and the emitter stack; and

implanting a dopant into the substrate that is exposed by the recess, wherein implanting results in a P-- collector tap, a P- collector tap, a P collector tap, a P+ collector tap, a P++ collector tap, an N-- collector tap, an N- collector tap, an N collector tap, an N+ collector tap, and an N++ collector tap.

7. (Original) The process according to claim 1, wherein forming the bipolar junction transistor between the first and second isolation structures includes:

in the substrate, forming an epitaxial layer;

forming a polysilicon film above the epitaxial layer; and

patterning the polysilicon film into emitter polysilicon.

8. (Original) The process according to claim 1, wherein forming the bipolar junction transistor between the first and second isolation structures includes:

in the substrate, forming an epitaxial layer;

forming a polysilicon film above the epitaxial layer;

patterning the polysilicon film into emitter polysilicon; and

forming a spacer on the emitter stack.

9. (Original) The process according to claim 1, wherein forming the bipolar junction transistor between the first and second isolation structures includes:

in the substrate, implanting a collector structure;

in the substrate, forming an epitaxial layer;

forming a polysilicon film over the epitaxial layer; and

patterning the polysilicon film into emitter polysilicon, wherein the emitter polysilicon is disposed above the collector structure.

10. (Original) The process according to claim 1, wherein forming an emitter stack includes:

in the substrate, forming an epitaxial layer;

forming a polysilicon film above the epitaxial layer;

patterning the polysilicon film into emitter polysilicon, wherein patterning the polysilicon film into emitter polysilicon further includes:

patterning a hard mask above the polysilicon film.

11. (Original) The process according to claim 1, wherein forming an emitter stack includes:

in the substrate, forming an epitaxial layer;

forming a dielectric layer above the epitaxial layer;

forming an emitter cut in the dielectric layer;

forming a polysilicon film above the epitaxial layer; and

patterning the polysilicon film into emitter polysilicon.

12. (Original) The process according to claim 1, further including:

in the substrate, forming a buried layer.

13- 26. (Canceled).